Amendments to the Specification

Please amend the specification as indicated.

Please amend paragraph [0002] as follows:

This application incorporates by reference U.S. Patent No. 6,525,955, entitled "Memory Cell With Fuse Element", U.S. Patent Application No. 10/038,021, filed on January 3, 2002 (now U.S. Patent No. 6,704,236 B2), U.S. Patent Application No. 10/041,296, filed on January 8, 2002 (now U.S. Patent No. 6,693,819 B2), and U.S. Patent Application No. 10/197,437, filed on July 18, 2002 (now U.S. Patent No. 6,700,176 B2).

Please amend paragraph [0008] as follows:

Accordingly, the present invention is directed to automatic programming time selection for one time programmable memory that substantially ~~obviates,~~ obviates one or more of the disadvantages of the related art.

Please amend paragraph [0009] as follows:

There is provided a method of programming a memory including the steps of attempting to program a bit at a designated address for a predetermined time; testing the bit to see if it has been programmed; increasing the predetermined time by approximately an order of magnitude; repeating the previous steps (until the bit at the designated address is ~~programmed;~~ programmed); and repeating all the previous steps by advancing the designated address until all bits in the memory are programmed.

Please amend paragraph [0015] as follows:

The programming of a bit in the OTP memory is done based on time. If a bit is programmed for time X (e.g., 10 μsec), and the tester returns a GOOD status, the programming of the bit is done. If the time X program cycle is complete, and the bit is not programmed correctly yet, the programming can be done again (and again) until it returns a GOOD status. The gate oxide barrier of the OTP memory will have lower and lower resistance with each programming attempt. ~~However~~ However, lab results show that if a bit fails the first attempt, the subsequent attempts must be longer in duration to reach success.

Please amend paragraph [0018] as follows:

FIG. 1 illustrates a flow diagram of the programming method of the present invention. As shown in **FIG. 1**, the programming apparatus waits for a program Start command (step **101**). Upon the Start command, a bit address is selected for programming (step **102**). If the address is equal to the previous address (step **103**), program time is increased (step **104**). The bit is then programmed (step **105**). On the next step, the status of the bit (Good or Bad) is returned to the tester (step **106**). The tester then returns back to step **101**. If, at step **103**, the address is not equal to the previous address, a short (i.e., default or standard) program time is selected (step **107**). The bit is then programmed (see step **105**, ~~etc.)~~ etc.).

Please amend the Abstract as follows on the next page: